WHAT IS CLAIMED IS

1. A method of marking an initial defective block in a semiconductor memory device having a memory area thereof divided into a plurality of blocks and provided with an ECC function, comprising the steps of:

detecting an initial defective block; and

writing an ECC code causing an ECC error in a predetermined area of the initial defective block.

2. The method as claimed in claim 1, wherein said step of writing an ECC code includes the steps of:

suspending an ECC generation function internal to said semiconductor memory device; and

writing the ECC code from an exterior of said semiconductor memory device.

3. The method as claimed in claim 1, further comprising the steps of:

reading data from the initial defective block after said step of writing an ECC code;

performing an ECC check on the read data; and

rejecting said semiconductor memory device as being defective if an ECC error is detected.

4. A method of searching for an initial defective block in a semiconductor memory device having a memory area thereof divided into a plurality of blocks and provided with an ECC function, comprising the steps of:

reading data from a predetermined area of a given block;

performing an ECC check on the read data;

identifying the given block as a defective block if an ECC error is detected.

5. A semiconductor memory device, comprising:

a memory area divided into a plurality of blocks;

an ECC generation circuit that generates an ECC code for data written in and data read from an accessed block; and

an ECC suspension circuit that suspends an ECC generation function of said ECC generation circuit so as to allow an ECC code to be directly written in said memory area from an exterior of the semiconductor memory device.

6. The semiconductor memory device as claimed in claim 5, wherein information about presence or absence of an ECC error is output to an exterior of the semiconductor memory device.

7. The semiconductor memory device as claimed in claim 6, wherein the information about presence or absence of an ECC error is output to the exterior of the semiconductor memory device in response to a predetermined command input after a data read operation.

8. The semiconductor memory device as claimed in claim 5, wherein information about whether ECC correction is possible is output to an exterior of said semiconductor memory device.

9. The semiconductor memory device as claimed in claim 8, wherein the information about whether ECC correction is possible is output to the exterior of said semiconductor memory device in response to a predetermined command input after a data read operation.